In support of his §112 rejections the Examiner has now remarked:

Claims 7-8: " it is not clear whether the terminals are covered or the wiring lines are covered. Only terminals are there on the outermost layers. Wiring lines are already covered by the insulating layers." [sic]

Claim 9: "it is not clear how spacing between two terminals will be 200 micrometer or more with a pitch of 100 micrometer of less." [sic]

Claims 10, 42: "it is not clear what is meant by "the conductive members in an area, over which the part is mounted, of the outermost layer of wiring lines connected with the connection terminals are arranged at a uniform density as a whole", and in particular, what is meant by "as a whole". There will be pads and traces on the top layer with different width and is not clear what kind of uniformity is there on the top layer. Further, what is 'conductive members?' Does it not include terminals, via the connections and traces?" [sic]

Claims 12, 44: "it is not clear what is meant by "conductive members in the area, over which the part is mounted, of each of the layers of wiring lines located below the outermost layer of wiring lines connect with the connecting terminals are arranged at a uniform density as a whole". Is it the spacing between the wiring identical on all layers or the shape/ width of wiring is identical on all the layers? Does the conductive member includes the via holes?" [sic]

Claims 15, 46: "it is not clear what is meant by "the conductive member at each of the layers of wiring lines below the outermost layer of wiring lines are arranged at substantially the same density as the density of the conductive members at the outermost wiring lines". Is it the identical wiring on all the layers or same material density on all the layers?" [sic]

Claims 53, 54: " it is not clear what is meant by "so as to be each located under a respective connecting terminal". Does it mean that the density is same and also the wiring lines are located under a respective connecting terminal? Examiner under the number of connecting terminals and number of wiring lines are same and the wiring lines are located under respective terminal on each layer below that of the connecting terminals." [sic]

It is well settled law that the claims of an application are to be interpreted in light of the specification and drawings. It is also well settled law that any technical terms not interpreted in light of the specification and drawings are to be taken in their ordinary sense, as defined in a Technical Dictionary or other defining publication.

It is well understood that the term pitch means: the distance between similar elements arranged in a pattern, or between two points of a mechanical part, as the distance between the peaks of two successive grooves on a disk recording or on a screw. *McGraw Hill Dictionary of Scientific and Technical Terms,* Sixth Edition at page 1604.

It is also well understood that the term density means: the total amount of quantity per unit of space. *McGraw Hill Dictionary of Scientific and Technical Terms,* Sixth Edition at page 572. One of ordinary skill in this area of art, Echigo et al. (USPN 6,274,821), cited by this Examiner in a divisional application hereto, addresses "density" at column 1, lines 27-36.

Claims 7-8 are clear on their face to one of ordinary skill in this art and recite:

> 7. (Original) The surface-mounting substrate of claim 1, wherein the connecting terminal is directly connected with the wiring line at the outermost layer in the surface-mounting substrate, and the wiring lines at the outermost layer are covered with a cover material.
>
> 8. (Original) The surface-mounting substrate of claim 7, wherein the cover material is a solder resist.

The Examiner's attention is also directed to Figs. 7-9, 12 and to the specification page 4, line 31 to page 5, line 9, page 12, lines 21-37, page 13, lines 10-25, and the abstract. One of ordinary skill would understand that the electrical connection terminals, which lie in the outermost layer have to be exposed to make electrical contacts with the projecting electrodes of a flip-chip semiconductor. One of ordinary skill also understands that underneath the terminal layer is a plurality of conductor layers made up of wiring patterns with interposed resin insulation. Since there are a number of wiring pattern layers on top of one another, there has to be an outermost one of these, i.e., the wiring pattern layer directly adjacent to terminal layer. This is clearly illustrated in the drawings and explained in the specification.

Claim 9 is clear on its face to one of ordinary skill in this art and is in accord with the accepted technical definition of the terms, as well as the illustrations in the drawings and the text of the specification. Claim 9 recites:

9. (Previously Amended) The surface-mounting substrate of claim 1, wherein the connecting terminals are arranged at a pitch of 100 micrometers or smaller and at a ~~spacing~~ distance between the terminals of 200 micrometers or larger.

With regard to claim 9 the Examiner is directed to Figs. 2, 6, 8. 10-11, and the specification page 5, lines 34 to page 6, line 19, page 6, lines 29-37, page 7, line1, page 12, lines 3-5, page 19, lines 33-37, page 20, line 1, and page 24, lines 5-15. One of ordinary skill in this art understands that "density" means number of wiring lines per micrometer. One of ordinary skill in this art also understands that a wire is a conductive member, i.e., a wiring line is a conductive member. One of ordinary skill in this art also understands that "pitch" is the space between lines. The "width" of a line is self-evident. Density, therefore, is a function of width and pitch. The Examiner is referred to US Pat. No. 6,274,821, as an example of the level of skill in this art and the understanding of these terms.

Claims 10 and 42 are clear on their face when read with the specification and in reference to the drawings. Claims 10 and 42 recite:

10. (Original) The surface-mounting substrate of claim 1, wherein conductive members in an area, over which the part is mounted, of the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

42. (Original) The structure of claim 40, wherein conductive members in an area, over which the part is mounted, of the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

From the drawings and specification identified above, it is readily understood by one of ordinary skill in this art, that "as a whole" means: "essentially uniform over the entirety of the area" or "practically uniform in that area" or any other meaning generally accepted in the art as an equivalent statement for "as a whole". The Examiner is reminded that an applicant is permitted to be his own lexicographer and that the meaning of his words are to be interpreted in light of his disclosure.

A reading of claims 12, 44 must be made in light of the disclosure. Claims 12 and 44 recite:

12.(Original) The surface-mounting substrate of claim 1, wherein conductive members in the area, over which the part is mounted, of each of the layers of wiring lines located below the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

44. (Original) The structure of claim 40, wherein conductive members in the area, over which the part is mounted, of each of the layers of wiring lines located below the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

From the discussion above, it is clear that one of ordinary skill understands the invention from the drawings and reading the specification. Claim 12 is clear on its face to say: for each of the layers of wiring lines below the outermost wiring line layer, the conductive members thereof (i.e., the "wires" in the wiring pattern of each sub-layer) are at a uniform density as a whole, for that region (area) of each sub-layer which is below the flip-chip.

Claim 12 and 44 depend from claim 1 and 40 respectively. Each of claims 1 and 40 recite the vias as separate elements, i.e., independent from the wiring pattern conductors (wiring lines). The claims 12 and 44 are therefore silent on the density of the vias.

Claims 15 and 46 recite as follows:

15. (Original) The surface-mounting substrate of claim 10, wherein the conductive members at each of the layers of wiring lines below the outermost layer of wiring lines are arranged at substantially the same density as the density of conductive members at the outermost wiring lines.

46. (Original) The structure of claim 42, wherein the conductive members at each of the layers of wiring lines below the outermost layer of wiring lines are arranged at substantially the same density as the density of conductive members at the outermost wiring lines.

From the discussion above, one of ordinary skill reading the specification and claims would readily understand that there are plural layers of wiring lines, with each wiring line layer consisting of a wiring pattern. Each successive layer of patterned wiring lines lies underneath the other layers as clearly shown in the drawings and recited in the claims. The outermost wiring line layer (12c - Figs. 2, 6) is obvious, it is the layer immediately under the terminal (10a) layer (see Figs. 2,6). The wiring line layers below layer 12c are layers 12b, 12a, where 12a is

not shown but understood to exist (see Fig. 6 as the example). The above-discussion has already made clear what one of ordinary skill in this art knows about "conductive members" of a layer of patterned wiring lines being the wires themselves. Likewise, "density" has been shown to be a well-known term of art.

New claims 53 and 54 recite different structure, but do not deviate from the terms of art of the previous claims, when they recite:

> 53. (Previously added) The surface-mounting substrate of claim 1, wherein the wiring lines of the respective wiring line layers below the connecting terminals are arranged at the same density as the density of connecting terminals so as to be each located under a respective connecting terminal.
>
> 54. (Previously added) The surface-mounting substrate of claim 40, wherein the wiring lines of the respective wiring layers below the connecting terminals are arranged at the same density as the density of connecting terminals so as to be each located under a respective connecting terminal.

The Examiner has questioned the phrase: "so as to be each located under a respective connecting terminal". However, the Examiner has stated that he understood that this phrase means that the number of connecting terminals and number of wiring lines are same and the wiring lines are located under respective terminal on each layer below that of the connecting terminal. [sic]

Applicant agrees with the Examiner's above-recited understanding as being consistent with the specification and drawings of the application.

In Summary Regarding § 112:

For all of the foregoing reasons the standing § 112 cannot be sustained and should now be withdrawn. Further in this regard, the standing rejection does not properly come under 35 USC 112, first or second paragraphs. The Examiner has not identified any portion of the specification or drawings which is unclear or which one skilled in the art will not understand (§112, first paragraph). Nor has the Examiner identified any antecedent issues (§112, second

aragraph.). Nor has the Examiner identified any language in the claims which is not found in the specification (§112, second paragraph). Lastly, the Examiner has not identified any claimed structure which is not illustrated in the drawings (§112, second paragraph.)

Remarks on new 35 USC 102 (b) and 103(a) rejections:

I) Claims 1,4,7,and 40 stand rejected under 35 USC 102(b) as anticipated by Arima et al. (US 5,375,042). In order for anticipation to be present, Arima must show each element claimed. This rejection is TRAVERSED.

Arima shows a thick film ceramic circuit board with a pair of thin film circuits disposed one on each of opposite surfaces of the thick film (circuit board). The thin film circuits of the assembly are formed of HEAT-RESISTING RESIN and a conducting material. [emphasis added in the form of a parenthesis and upper case letters].

Arima's design focus is to solve his warping problem. Specifically, Arima states at column 3, lines 50-61:

> "Further, if a thin film circuit was formed on only one surface of the substrate assembly in the semiconductor package as conventional, the substrate assembly would have been curved, i.e., warped into a curved shape due to the difference in coefficient of linear expansion between the organic insulating film of the thin film circuit and the ceramic circuit board. In this invention, since a pair of thin film circuits are formed one on each of the opposite surfaces of the substrate assembly to cancel each other's influence, it is possible to minimize curving." [emphasis added]

Arima is not concerned with nor does it anticipate the same problem as the current invention. One reason is because Arima uses a "heat-resisting resin". A second reason is that he never addresses nor does he indicate he even considers exceeding the glass transition temperature (t_g) of his resin. Lastly, Arima does not consider a problem created in production, but in later use. If there is no heat applied to his production device (or conversely, cold) there the respective films would not expand or contract at different degrees. They would stay flat as they are when manufactured.

Warping is the formation of a gradual curvature, i.e., a bowing of the film structure when the expansion of the outer thin film differs from the inner thick film (with only one side covered). This expansion occurs when the device is subjected to the ambient heat of a computer, controller or other device installation, i.e., in later use.

Furthermore, Arima's structure departs drastically from that shown and claimed in the present application by applicant. Arima uses a connecting pad 7, which is part of his semiconductor chip 6. He uses solder 8 to connect his chip to a connecting pad 5 (connecting terminal) on his board. Directly underneath Arima's connecting terminal layer (19) of connecting pads 5, is a vertical wiring layer 18 (extending in the "Y" direction). See column 5, lines 8-12 and column 6, lines 56-57. Underneath Arima's "Y" direction layer 18 is a horizontal layer (extending in the "X") direction. See column 5, lines 6-8, column 6, lines 55-56, and column 9, lines 20-23.

Since Arima is concerned with "warping" he is solving his "warping" problem with plywood, not actual plywood, but with cross-axis construction identical to how plywood is made. Generally, plywood does not warp. Of course the Arima constuction is balanced. He has a "core" with two "cross-plies" on either side of his core.

Each of Arima's layers has conductive members (his copper conductors) and connecting via holes. While Arima does not recite if any of his vias in vertical layer 18 or underneath horizontal layer 17 are filled he does recite that the vias 12 in his ceramic board 1 are filled with tungsten paste. See column 4, lines 58-59, column 5 and column 6, lines 45-46.

Contrary to Arima, applicant neither shows nor claims "vertical" layers. Applicant expressly shows and claims that each of his layers of patterned wiring lines are similar if not identical, and does not show nor claim a "vertical" layer, nor any cross-plies for applicant's layers. See applicants Figs. 2, 4, and 17 for illustrations. The respective pages and lines of the specification need not be cited here.

For these reasons, the standing 35 USC 102(b) rejection of claims 1,4, 7, and 40 cannot be sustained and should now be removed.

II) Claims 8-15, 18-24 and 42-46 stand rejected under 35 USC 102(b) as obvious when read in light of Arima et al. (US 5,375,042). In order for obviousness to be present, Arima must show each element claimed prior element claimed, and those additional elements introduced in these additional claims, must be obvious to one of ordinary skill in the art to introduce these additional claimed elements, after reading Arima. This rejection is TRAVERSED.

These claims depend from previous claims which should now be considered allowable. Therefore, these additional dependent claims 8-15, 18-24 and 42-46 must also be considered allowable. However, with respect to claim 8, one of ordinary skill in the art would never introduce a solder resist layer on the topmost surface. One of ordinary skill recognizes that Arima has built a balanced two cross-ply structure. Adding any material destroys the balance, introduces additional discrepancies in expansion and defeats the purpose of Arima's structure.

Likewise, respect to claim 9 regarding "terminal" pitch, and claims 10, 12,15, 42, 44 and 46, and claims 19-24, regarding arrangement of terminals, wiring lines on the top surface and below the top surface, and spacing of terminals, wiring lines, vias, etc. Any change to the Arima balanced physical structure, spacing, introduction of dissimilar material, change in relationships of metal to resin to paste etc., must of necessity change the coefficient of expansion of the Arima various layers and defeat the Arima balanced design to stop "warping". This portion of this rejection is untenable.

Regarding claims 14 and 18, the introduction of a power layer or a ground layer to the Arima, accordingly will change the balance between the top cross-plies and the bottom cross-plies, introduce different coefficients of expansion and defeat Arima's design. One of ordinary skill would never consider the changes suggested by the Examiner.

Arima cannot be changed to include the structure recited in applicants claims 8-15, 18-24 and 42-46 with significant further engineering and invention. Even such significant further engineering and design, there is no guarantee the redesign of the Arima as suggested by the Examiner would produce an operative design which would not warp, as is required by Arima.

For these reasons, the standing 35 USC 103 (a) rejection of claims 8-15, 18-24 and 42-46 should now be withdrawn.

III) Claims 16, 17 and 41 stand rejected as obvious under 35 USC 103(a) in view of Arima when read with Hsu et al. (USPN 6,242,815). This rejection is TRAVERSED.

Hsu is relied upon for the showing of dummy pads or wiring . However, this is not quite what Hus shows. What Hsu shows is a "dummy connection pad" centrally disposed on his flexible film to add structural rigidity to that film. See column 2, lines 10-15, 29-34. Hsu uses this "dummy" as a stiffener to keep his film from flexing in use and thereby reducing "die cracking or delamination". Hsu places a layer of cupric oxide on the surface of his "dummy". See column 3, lines 48-50 and column 4, lines 22-23. Moreover, Hsu teaches that his dummy pads can be "bar-like, oval-shaped or circular" (column 3, lines 48-49). Hsu is not concerned with shape because he is not concerned with coefficient of expansion.

Moreover, Hsu is not concerned with excessive manufacturing heat for any underlying layer and therefore places his "dummy" in his terminal layer and does not suggest any other location. For the reasons above-recited, one of ordinary skill would not disturb the surface layer 19 of Arima, or Arima's vertical wiring layer 18, or Arima's horizontal wiring layer 17, without defeating Arima's design. One of ordinary skill would know this and never apply the references as suggested by the Examiner.

Lastly, these claims 16, 17 and 41 depend from what is now to be considered as allowable claims and therefore are likewise to be considered allowable. The standing 35 USC 103(a) rejection of claims 16, 17 and 41 should now be withdrawn.

In the Claims:

Amend claims to recite as follows as follows. The claims are presented pursuant to the newly revised requirements of 37 CFR 1.121.

1.(Previously Amended) A surface-mounting substrate for mounting a part thereon, which comprises a core substrate, a plurality of layers of patterned wiring lines, which are separated from each other by an insulation layer interposed therebetween, vias piercing through the insulation layer to connect the wiring lines at the adjacent layers to each other, and a layer of connecting terminals to mount a part on the surface-mounting substrate, each of the connecting terminals connecting with the wiring line at the outermost layer of wiring lines, wherein the connecting terminal is filled in an outermost insulation layer provided at the surface of the surface-mounting substrate, and has a surface exposed at substantially the same level as the level of the surface of the outermost insulation layer, the connecting terminal being provided on its surface with solder material.

2. (Deleted)
3. (Deleted)

4. (Original) The surface-mounting substrate of claim 1, wherein the part to be mounted is a semiconductor device.

5. (withdrawn/ elected out)
6. (withdrawn/ elected out)

7. (Original) The surface-mounting substrate of claim 1, wherein the connecting terminal is directly connected with the wiring line at the outermost layer in the surface-mounting substrate, and the wiring lines at the outermost layer are covered with a cover material.

8. (Original) The surface-mounting substrate of claim 7, wherein the cover material is a solder resist.

9. (Twice Amended) The surface-mounting substrate of claim ~~1~~ 53, wherein the connecting terminals are arranged at a pitch of 100 micrometers or smaller and at a distance between the terminals of 200 micrometers or larger.

10. (Amended) The surface-mounting substrate of claim ~~1~~ 53, wherein conductive members in an area, over which the part is mounted, of the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

11. (Original) The surface-mounting substrate of claim 10, wherein the conductive members include the wiring lines and the connecting terminals.

12.(Amended) The surface-mounting substrate of claim ~~1~~ 53, wherein conductive members in the area, over which the part is mounted, of each of the layers of wiring lines located below the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

13.(Original) The surface-mounting substrate of claim 12, wherein the conductive members include the wiring lines and the vias.

14. (Original) The surface-mounting substrate of claim 13, wherein the conductive members further include a power supply plane and/or a grounding plane.

15. (Original) The surface-mounting substrate of claim 10, wherein the conductive members at each of the layers of wiring lines below the outermost layer of wiring lines are arranged at substantially the same density as the density of conductive members at the outermost wiring lines.

16. (Original) The surface-mounting substrate of claim 10, which has dummy members at at least one of layers of wiring lines.

17. (Original) The surface-mounting substrate of claim 12, which has dummy members at at least one of layers of wiring lines.

18. (Original) The surface-mounting substrate of claim 14, wherein the power supply plane and/or the grounding plane is in a mesh-like shape or has slits.

19. (Original) The surface-mounting substrate of claim 10, wherein the wiring lines have a width of 20 to 200 micrometers, and are arranged at a pitch of 60 to 300 micrometers.

20. (Original) The surface-mounting substrate of claim 12, wherein the wiring lines have a width of 20 to 200 micrometers, and are arranged at a pitch of 60 to 300 micrometers.

21. (Original) The surface-mounting substrate of claim 10, wherein the vias have a diameter of 0.05 to 0.6 millimeter.

22. (Original) The surface-mounting substrate of claim 12, wherein the vias have a diameter of 0.05 to 0.6 millimeter.

23. (Original) The surface-mounting substrate of claim 10, wherein the core substrate has through holes to connect a wiring line at one side of the substrate to another wiring line at the other side, the through holes having a diameter of 0.2 to 0.6 millimeter, and being arranged in a pitch of 0.5 to 1.5 millimeters.

24. (Original) The surface-mounting substrate of claim 12, wherein the core substrate has through holes to connect a wiring line at one side of the substrate to another wiring line at the other side, the through holes having a diameter of 0.2 to 0.6 millimeter, and being arranged a pitch of 0.5 to 1.5 millimeters.

25. (withdrawn/ elected out)

26. (withdrawn/ elected out)
27. (withdrawn/ elected out)
28. (withdrawn/ elected out)
29. (withdrawn/ elected out)
30. (withdrawn/ elected out)
31. (withdrawn/ elected out)
32. (withdrawn/ elected out)
33. (withdrawn/ elected out)
34. (withdrawn/ elected out)
35. (withdrawn/ elected out)
36. (withdrawn/ elected out)
37. (withdrawn/ elected out)
38. (withdrawn/ elected out)
39. (withdrawn/ elected out)

40. (Previously Amended) A structure comprising a surface-mounting substrate and a part mounted thereon, the surface-mounting substrate comprising a core substrate, a plurality of layers of patterned wiring lines, which are separated from each other by an insulation layer interposed therebetween, vias piercing through the insulation layer to connect the wiring lines at the adjacent layers to each other, and a layer of connecting terminals to mount the part on the surface-mounting substrate, each of connecting terminals connecting with the wiring line at the outermost layer of wiring lines, and the part having bumps, and being mounted on the substrate through the bumps bonded to the respective connecting terminals, wherein the connecting terminal of the surface-mounting substrate is filled in an outermost insulation layer provided at the surface of the surface-mounting substrate such that the entire surface of a connecting terminal is exposed at the surface of the mounting substrate, and has a surface exposed at substantially the same level as the level of the surface of the outermost insulation layer, the connecting terminal being provided on its surface with solder material.

41. (Previously Amended) The structure of claim 40, wherein the part to be mounted is a semiconductor device and wherein at lest one of said layers of patterned wiring lines is a dummy layer.

42. (Original) The structure of claim 40, wherein conductive members in an area, over which the part is mounted, of the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

43. (Amended) The structure of claim ~~42~~ 54, wherein the conductive members include the wiring lines and the connecting terminals.

44. (Amended) The structure of claim ~~40~~ 54, wherein conductive members in the area, over which the part is mounted, of each of the layers of wiring lines located below the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole.

45. (Original) The structure of claim 44, wherein the conductive members include the wiring lines and the vias.

46. (Original) The structure of claim 42, wherein the conductive members at each of the layers of wiring lines below the outermost layer of wiring lines are arranged at substantially the same density as the density of conductive members at the outermost wiring lines.

47. (withdrawn/ elected out)
48. (withdrawn/ elected out)
49. (withdrawn/ elected out)
50. (withdrawn/ elected out)
51. (withdrawn/ elected out)
52. (withdrawn/ elected out)

53. (Amended) A surface-mounting substrate for mounting a part thereon, which comprises a core substrate, a plurality of layers of patterned wiring lines, which are separated from each other by an insulation layer interposed therebetween, vias piercing through the insulation layer to connect the wiring lines at the adjacent layers to each other, and a layer of connecting terminals to mount a part on the surface-mounting substrate, each of the connecting terminals

connecting with the wiring line at the outermost layer of wiring lines, wherein the connecting terminal is filled in an outermost insulation layer provided at the surface of the surface-mounting substrate, and has a surface exposed at substantially the same level as the level of the surface of the outermost insulation layer, the connecting terminal being provided on its surface with solder material ~~The surface-mounting substrate of claim 1~~, wherein the wiring lines of the respective wiring line layers below the connecting terminals are arranged at the same density as the density of connecting terminals so as to be each located under a respective connecting terminal.

54. (Amended) A structure comprising a surface-mounting substrate and a part mounted thereon, the surface-mounting substrate comprising a core substrate, a plurality of layers of patterned wiring lines, which are separated from each other by an insulation layer interposed therebetween, vias piercing through the insulation layer to connect the wiring lines at the adjacent layers to each other, and a layer of connecting terminals to mount the part on the surface-mounting substrate, each of connecting terminals connecting with the wiring line at the outermost layer of wiring lines, and the part having bumps, and being mounted on the substrate through the bumps bonded to the respective connecting terminals, wherein the connecting terminal of the surface-mounting substrate is filled in an outermost insulation layer provided at the surface of the surface-mounting substrate such that the entire surface of a connecting terminal is exposed at the surface of the mounting substrate, and has a surface exposed at substantially the same level as the level of the surface of the outermost insulation layer, the connecting terminal being provided on its surface with solder material ~~The surface-mounting substrate of claim 40~~, wherein the wiring lines of the respective wiring layers below the connecting terminals are arranged at the same density as the density of connecting terminals so as to be each located under a respective connecting terminal.

REMARKS

The Examiner has remarked that previously added new claims 53 and 54 would be allowable to overcome the 35 USC 112 rejections. Applicant asserts that the above-cited response asserts that the 35 USC 112, second paragraph rejection(s) should now be withdrawn. In this regard, should the Examiner have any remaining issue with claims 53, 54, he is respectfully requested to telephone applicant's attorney to hopefully resolve any remaining use by telephone conference.

Claims 53 and 54 previously depended from claims 1 and 40, respectively, and have now been amended herein into independent form. Claims 9-20 have been amended to depend from what is now believed to be allowable claim 53. Claims 43-46 have been amended to depend from what is now believed to be allowable claim 54.

Claims 1, 4-8 and 40-42 remain as previously examined. In light of the above-recited remarks it is urged that claims 1, 4-8 and 40-42 distinguish applicant's invention over Arima and over Arima when read with Hsu. The Examiner's remarks titled : "Conclusion" have been disregarded with respect to his remarks on "Andou et al., Iijima et al., Tanaka, Goodman et al., Hirano and Schaper. These references are not relied upon in any rejection. It is presumed that the Examiner has recited them in his remarks to remind the applicant not to amend his claims away from Arima and Hsu, but into these additional references.

It is requested that the application be reexamined as to the claims 1, 4, 7-24, 40-46 and 53, 54 and be passed to issue with these claims.

Respectfully submitted,
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